500.38532CX1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	K. OSADA, et al.
Application No.:	10/606,954
Filed:	June 27, 2003
For:	SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE
Art Unit:	Unknown
Examiner:	Unknown

SUPPLEMENTAL REQUEST FOR RECONSIDERATION

Commissioner for Patents
P.O. BOX 1450
Alexandria, VA 22313-1450

August 18, 2003

Sir:

In supplement to the preliminary amendment filed on June 27, 2003, reconsideration and allowance of newly submitted claims 1-18 is respectfully requested.

As noted in the Preliminary Amendment, new claims 1-15 correspond to claims 31-37, 45-50, 2 and 3 of the parent application serial number 09/565,535. Specifically, claims 1-7 of the present application correspond to claims 31-37 of the parent case. Claim 8-13 correspond to claims 45-050 of the parent case, and claims 14 and 15 of the present application correspond, respectively, to claims 2 and 3 of the parent case.

In the Final Office Action in the parent application, claims 45-50 (presently claims 8-13) were not considered because they were regarded as not being directed to the elected embodiment of Figs. 4 and 5. The reason given in the Final Office

Action (dated February 11, 2003) was that Figs. 4 and 5 do not show isolation of first and second active regions from one another by an isolation layer. Claims 31-37, 2 and 23 (present claims 1-7, 14 and 15) were rejected under 35 U.S.C. § 112, first paragraph, on the basis that Figs. 4 and 5 don't show the claimed feature of "an outer shape of the diffusion layer defined by an isolation layer extending along the entirety of each of the longitudinal sides of the diffusion layer." Claims 31-37, 2 and 3 were also rejected over prior art, apparently without considering the above quoted limitation regarding the isolation layer.

In response, Applicants respectfully request consideration of all of the claims 1-15 and removal of the 35 U.S.C. § 112, first paragraph and prior art rejections regarding these claims. In particular, it is respectfully requested that the Examiner consider all of these claims as an embodiment which includes the memory cells of Figs. 4 and 5 taken within the overall context of a memory array such as shown in Fig. 3. Specifically, when one considers Figs. 4 and 5 within such an array as shown in Fig. 3, the recited isolation layer is, in fact, supported. As will be discussed in detail below, considering Figs. 4 and 5 within the overall context of the memory array of Fig. 3 serves to overcome both the 35 U.S.C. § 112, first paragraph, rejection and the prior art rejection set forth in the February 11, 2003 Office Action in the parent case. It also serves to eliminate the reason for not considering claims 8-13 together with claims 1-7, 14 and 15.

Concerning the configuration of Figs. 4 and 5 as part of an array in general, it is noted that the specification clearly indicates the intention that all of the illustrated memory cell embodiments be considered as part of a memory array. This is reflected, for example, on page 7, line 21 et seq. which states:

> "In accordance with a still another aspect of the invention, memory cells are laid out into the form of an array, wherein contacts

to a substrate to a p-type well region and a contact to a substrate of an n-type well region are linearly disposed within the array and at upper and lower portions of the array in a direction parallel to the word lines."

Page 8, line 6 et seq. also defines the invention in terms of:

"In accordance with yet another aspect of the invention, a semiconductor device is provided which comprises a plurality of memory arrays, each including an array of memory cells having at least...."

The original abstract also refers to the use of the invention (which would include all of the embodiments, including the embodiment of Figs. 4 and 5) within an array. Specifically, the last sentence of the abstract states:

"At intermediate locations of an array, regions for use in supplying power to the substrate are formed in parallel to word lines in such a manner that one regions is provided per group of 32 memory cells rows or 64 cells rows."

Still further, page 14, line 19 et seq. states:

"In case the memory cells are laid out into the form of an array, the diffusion layers become four separate straight lines extending parallel to the bit lines (BL1, BL2)."

In other words, it is respectfully submitted that one of ordinary skill in the art reading the specification is clearly advised that, although embodiments are shown in terms of specific memory cell structure, in each case these specific memory cells are clearly intended to be used within memory arrays.

With regard to Fig. 3 itself, it is stated on page 16, line 19 et seq. that:

"Turning to Fig. 3, an exemplary case is shown where the memory cells MC of embodiment 1 are laid out into the form of an array."

Line 24 et seq. goes on to reiterate that "the memory cells MC are organized into an array of 256 rows and 128 columns, by way of example." In other words, the specification advises the reader to add the memory cells of the embodiment 1 (e.g. Figs. 1 and 2) into Fig. 3 so that the memory array of Fig. 3 can be understood as including specific memory cells such as those shown in embodiment 1.

Turning to the embodiment 3 shown in Figs. 4 and 5, it is stated on page 19, lines 4 et seq.:

> "Memory cell MC2 of embodiment 3 is similar to the memory cell MC of embodiment 1, with the exception that, as compared to embodiment 1,..."

As such, it is clear that embodiment 3 (Figs. 4 and 5) is simply a modification of embodiment 1, with some adjustments being made regarding shape. And, as noted above, the specification and abstract clearly imply that the memory cells of all of the memory cell embodiments are intended to be utilized in memory arrays. Since Fig. 3 is the only memory array actually shown in the specification, it is respectfully submitted that it would be clear to one of ordinary skill in the art that embodiment 3 of Figs. 4 and 5 should be considered in the context of the memory array shown in Fig. 3. In other words, similar to the direction of page 16, line 19 et seq. to incorporate the memory cells of Figs. 1 and 2 within the memory array of Fig. 3, one of ordinary skill in the art would also be led to consider the memory cells of embodiment 3 (Figs. 4 and 5) within the context of the memory array of Fig. 3.

To put this another way, one of ordinary skill in the art would not consider Figs. 4 and 5 in a vacuum without correlating them to a memory array. And, since the specific memory array shown in the specification is Fig. 3, it would be logical to incorporate the Fig. 4/Fig. 5 memory cells into the memory array of Fig. 3. This is particularly the case since page 19, line 43 et seq. equates the memory cells of the

Fig. 4/Fig. 5 embodiment to the memory cells of the Fig. 1/Fig. 2 embodiment. Therefore, it is respectfully requested that the Examiner consider the embodiment of the memory cells of Figs. 4 and 5 as part of the array shown in Fig. 3, rather than simply as an isolated memory cell structure separate from any array.

Once the memory cells of Figs. 4 and 5 are considered as part of the memory array of Fig. 3, it becomes clear that there is, in fact, support for the language of claim 1 of:

> "Wherein an outer shape of the diffusion layer, defined by an isolation layer which extends along the entirely of each of the longitudinal sides of the diffusion layer, it substantially linearly symmetric...."

Specifically, this isolation region is shown between the edge of the well PW1 of Fig. 3 and the boundary of the adjacent memory cells. As shown in Fig. 3, there are no additional diffusion regions between the edges of the well PW1 of each of the memory cells and the boundary with an adjacent memory cell. Therefore, when Figs. 4 and 5 are considered within the context of the memory cell of Fig. 3, the claim language of claim 1 is supported. Therefore, reconsideration and removal of the 35 U.S.C. § 112, first paragraph, rejection set forth in the February 11, 2003 Office Acton in the parent case is respectfully requested.

Once this limitation regarding the isolation region in claim 1 is considered, the prior art rejection based on USP 5,930,163 to Hara and USP 5,072,286 to Minami is also overcome. Specifically, neither Hara nor Minami, wither considered alone or in combination, teach or suggest this claim structure with the isolation region in combination with the other elements recited in the claim. Therefore, reconsideration and allowance of claims 1-7, 14 and 15 corresponding to claims 31-37, 2 and 3 of the parent application, is respectfully requested.

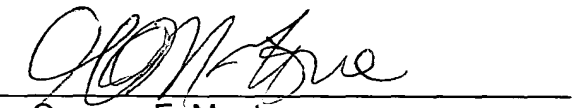
Finally, in considering the memory cell structure of Figs. 4 and 5 in the context of the memory array of Fig. 3, consideration and allowance of claims 8-13 is also respectfully requested. Specifically, when these figures are considered together, the claimed isolation region is provided for the embodiment of Figs. 4 and 5. Therefore, consideration of claims 8-15, together with claims 1-7, 14 and 15 is respectfully requested.

If the Examiner believes that there are any other points which may be clarified or otherwise disposed of, either by telephone discussion or by personal interview, the Examiner is invited to contact applicants' undersigned attorney at the number indicated below.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit account of Antonelli, Terry, Stout & Kraus, Deposit Account No. 01-2135 (500.38532CX1).

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

By 

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